**Implementation of Bus Bridge between AHB and OCP**

**Abstract**

Protocols are commonly used today to connect IP blocks on structured SoCs. Generally  
Protocol is the back-bone of the SoC and its failure usually leads to a non-functional chip. In  
present market, various types of standard protocols are available and are used in SoC  
which requires a bridge to pass the information from one type of protocol to other type of  
protocol safely and without any data loss. Open Core Protocol (OCP) and AMBA – Advanced  
High Performance Bus (AHB) protocol are standard and commonly used protocols. In this  
work, the bus bridge was designed to interface these protocols which plays a vital role in SoC  
application such as it may lead to application failure, if it doesn’t work properly. Initially basic  
OCP and AHB protocols are modeled separately using VHDL and are simulated. Basically Bus  
Bridge should convert command and data of OCP formats to acceptable AHB formats. This conversion does not ensure proper communication unless the timings of each protocol were met. Hence the interconnecting Bus Bridge wrapper between Core Centric Protocol (OCP) and Bus Centric Protocol (AHB) was designed with proper timing delay. The simulation results obtained were analyzed to adjust the timing of the design. Overall timing of various signals present in the design was optimized to meet the design objectives.

**LANGUAGE USED:**

* Vhdl/verilog

**TOOLS REQUIRED:**

* MODELSIM – Simulation
* XILINX-ISE – Synthesis